

REMARKS

Claims 1 - 25 remain active in this application. New claims 26 - 36 have been added to more fully claim the subject matter regarded as the invention. Claims 1, 8 - 22 and 24 - 25 have been amended to improve form and emphasize meritorious effects of the invention. Support for the amendments of the claims and new claims is found throughout the application, particularly in Figures 3, 4, 6, 7, 9 and 10 and the description thereof in regard to zero voltage mode switching on pages 7 - 13. The circuit configuration recited in new claim 36 is illustrated in Figures 5 and 8, also described on pages 7 - 13. No new matter has been introduced into the application.

Claims 1, 5 - 7, 15 and 19 - 25 (and, apparently, claims 2 - 4, 16 - 18 and 23 - 25) have been rejected under 35 U.S.C. §103 as being unpatentable over Chida in view of the admitted prior art and Vinciarelli et al. Claims 8 - 14 have been rejected under 35 U.S.C. §103 as being unpatentable over Chida in view of the admitted prior art, Vinciarelli et al. and Nakagawa et al. Both of these grounds of rejection are respectfully traversed. It is respectfully submitted that the application of prior art by the Examiner is clearly an attempted hindsight reconstruction by, in essence, addition of individual features to the admitted prior art from very different circuits and where the elements have very different functions therein.

Specifically, Chida is directed to boost (Figures 5, 7, 9 and 11), buck (Figure 12) or boost/buck (Figure 13) quasi-resonant power converters operating in a full wave mode and which thus necessarily includes a diode in the output circuit thereof and which have only one switch. The problem with which Chida is concerned is the storage of energy in the parasitic capacitance of

the switch while the switch is off and the energy trapped by the diode. Therefore, the energy must be "internally" dissipated while the switch is on (column 1, lines 30 - 40); rendering such circuits impractical for high frequency operation prior to Chida since this type of loss increases with frequency of operation. As a solution, Chida forms the (single) switch using a pair of back-to-back MOSFETs which are connected in series such that their internal parasitic diodes are oppositely poled and which are controlled such that both MOSFETs are simultaneously turned on or turned off (column 3, lines 52 - 58). By doing so, the parasitic diode of one transistor discharges the parasitic capacitor of the other during respective half-waves of the resonant oscillation. No such diode is required in the types of power converters (e.g. half-wave mode) to which the invention is directed and in which multiple switches are used to develop the desired voltage at high current as clearly recited in the claims. While the invention of Chida is evidently applicable to a buck converter, the buck converter of Figure 12 effectively includes on one switch (most closely corresponding to the claimed top switch in series with the voltage supply) and operated in a much different manner from the admitted prior art as well as the present invention. Moreover, Chida is directed to full-wave quasi-resonant converters and thus teaches away from half-wave quasi-resonant operation of the admitted prior art (by which the Examiner appear to attempt to reconcile Chida with the present invention) and the present invention and, by the same token, there can be no motivation for inclusion of the switch circuit of Chida in a half-wave quasi-resonant converter circuit since voltage across the resonant capacitor would then be unipolar rather than bipolar (see column 1, lines 18 - 29) and the switch circuit of Chida is specific to solving a problem which arises

only from bipolar quasi-resonant operation.

These deficiencies of Chida and the admitted prior art are not mitigated by Vinciarelli et al. or Nakagawa and, again, these references are so different in operation from Chida and the admitted prior art that the combination of teachings asserted by the Examiner is improper. Specifically, the switches of the various embodiments of Vinciarelli et al. operate in a zero current switching (ZCS) mode whereas Chida and at least the auxiliary switch and the synchronous switch of the invention operate in a zero voltage switching (ZVS) mode. ZCS and ZVS are totally different modes of operation and it is clear that the switches of Vinciarelli must be turned on while having a voltage imposed across them. Nevertheless, the invention also provides the additional advantage of being operable with near-zero current switching which is not available together with zero voltage switching in either Chida or Vinciarelli et al. and these references and the admitted prior art do not lead to an expectation of success in achieving such a meritorious effect.

Similarly, Nakagawa (which has been applied only in regard to the tap-buck embodiment of the invention having a tapped inductor) operates in a much different manner from the invention. As explicitly recited beginning at column 4, line 54, switch 104 of Figure 2 is an active clamp "for conducting a soft switching operation" (as an alternative to lossless snubber circuits used for the same purpose) whereas, in the present invention, the switching points are chosen relative to the resonant period such that ZVS is achieved. This matching of switching points to the resonant period also allows exploitation of resonance with both the auxiliary inductance (not taught by Nakagawa) and the leakage inductance of the tapped inductor to extend the conduction period. Therefore, Nakagawa does not mitigate the deficiencies of Chida,

the admitted prior art and Vinciarelli et al. taken in any combination.

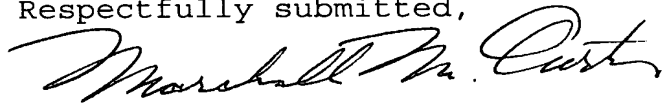
Accordingly, it is respectfully submitted that the grounds of rejection asserted by the Examiner are in error and untenable and amount to an impermissible attempted hindsight reconstruction of the invention. It has been demonstrated that the teachings and suggestions of the prior art relied upon by the Examiner are not properly combinable and even if properly combinable, do not provide evidence of a level of ordinary skill in the art which would support the conclusion of obviousness that the Examiner has asserted. By the same token, the Examiner has not made a *prima facie* demonstration of obviousness of the subject matter of any claim. Nevertheless, the claims have been amended to recite that particular switches are operated using ZVS which are neither taught nor suggested by the prior art (e.g. Chida mentions ZVS but does not disclose a synchronous switch distinct from but in combination with other switches which are operated using ZVS, ZVS is not admitted to be known for operation of the circuits of prior art Figures 1 and 2, Vinciarelli et al. uses ZCS but not ZVS, Nakagawa operates switches 103 and 104 differently from the present invention for a different purpose and does not appear to include a resonant auxiliary inductance, etc.). Therefore it is respectfully submitted that claims 1 - 25 are all clearly patentably distinct from the prior art. Similar recitations are contained in new claims 26 - 36 which are believed to be distinct from the prior art for the same reasons. Therefore, reconsideration and withdrawal of the asserted grounds of rejection are respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully

submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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